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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,381	06/29/2004	Masatake Nakano	120164	9028

25944 7590 06/16/2005

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
ISAAC, STANETTA D	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/500,381	NAKANO, MASATAKE	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 7-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 7-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed on 6/29/04. Currently, claims 7-22 are pending.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The information disclosure statement (IDS) was submitted on 6/ 29/04. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 7-22 are rejected under 35 U.S.C. 102(a)/(e) as being anticipated by Inazuki et al. US Patent 6,362,076.

Inazuki discloses the semiconductor method as claimed. See figures 1-4, and corresponding text, where Inazuki teaches, pertaining to claim 7, a method of producing an SOI wafer comprising at least the steps of forming an insulator film **3** on at least one of a bond wafer **2** made of silicon single crystal to form an SOI layer and a base wafer **1** made of silicon single crystal to be a support substrate (figure 1; col. 4, lines 45-56), bonding each main surface of the bond wafer and the base wafer via the insulator film (figure 1; col. 4, lines 64-67; col. 5, lines 1-3), and making the bond wafer bonded to the base wafer thinner, wherein one silicon wafer selected from a group consisting of an epitaxial wafer, and FZ wafer, a nitrogen doped wafer, a hydrogen annealed wafer, an intrinsic gettering wafer, a nitrogen doped and annealed wafer, and an entire N-region wafer is used as the base wafer (figure 1; col. 5, lines 17-27; col. 6, lines 39-45, epitaxial or FZ wafers).

Inazuki teaches, pertaining to claim 8, a method of producing an SOI wafer comprising at least the steps of forming an insulator film **3** on at least one of a bond wafer **2** made of silicon single crystal to form an SOI layer and a base wafer **1** made of silicon single crystal to be an support substrate (figure 1; col. 4, lines 45-56), forming a micro bubble layer in the bond wafer

by implanting gas ions from a main surface of the bond wafer (figure 1; col. 4, lines 57-63), bonding the ion-implanted main surface of the bond wafer to a main surface of the base wafer via the insulator film (figure 1; col. 4, lines 64-67; col. 5, lines 1-3) , and delaminating the bonded wafer at the micro bubble layers as a border, wherein one silicon wafer selected from a group consisting of an epitaxial wafer, an FZ wafer, a nitrogen doped wafer, a hydrogen annealed wafer, an intrinsic gettering wafer, a nitrogen doped wafer, a hydrogen annealed wafer, an intrinsic gettering wafer, a nitrogen doped and annealed wafer, and an entire N-region wafer is used as the base wafer (figure 1; col. 5, lines 4-35; col. 6, lines 39-45 epitaxial and FZ wafers).

Inazuki teaches, pertaining to claims 9 and 10, wherein one silicon wafer selected from a group consisting of an epitaxial wafer, an FZ wafer, a nitrogen doped wafer, a hydrogen annealed wafer, an intrinsic gettering wafer, a nitrogen doped and annealed wafer, and an entire N-region wafer is used as the bond wafer (col. 6, lines 39-45).

Inazuki teaches, pertaining to claims 11 and 12 , wherein the SOI layer to be formed has a thickness of 0.3 μm or less. In addition, Inazuki teaches, pertaining to claims 13-18, wherein the SOI layer to be formed has a thickness of 0.3 μm or less (col. 4, lines 11-15). Also, Inazuki teaches, pertaining to claims 19-22, an SOI wafer produced by the method according to claims 7-10 (figure 1; col. 5, lines 36-41).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
June 9 2005

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812